

## ABSTRACT:

A multiprocessor array with a first shadow register unit (3) which operates within a first clock domain, at least one second shadow register unit (11) which operates within a second clock domain, and a peripheral unit (17) which operates within a peripheral clock domain. Within all clock domains there are provided register units (3, 11, 20) which  
5 have a construction that is functionally identical.

Fig. 1

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